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(71) Applicant:  
STMicroelectronics S.r.l.  
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:  
• Murari, Bruno  
20052 Monza (IT)

• Ferrari, Paolo  
21013 Gallarate (IT)  
• Vigna, Benedetto  
85100 Potenza (IT)

(74) Representative:  
Cerbaro, Elena et al  
STUDIO TORTA S.r.l.,  
Via Viotti, 9  
10121 Torino (IT)

### (54) Process for manufacturing integrated microstructures of single-crystal semiconductor material

(57) The process comprises forming a buried sacrificial layer (5) of porous silicon in the starting substrate (2) and then a single-crystal epitaxial layer (7) intended to accommodate both the sensitive element and the integrated circuit. After forming electronic components (12, 18) in the epitaxial layer, the epitaxial layer (7) is anisotropically etched over the buried sacrificial layer (5) to form trenches (27) through which the buried sacrificial layer is then etched and removed. The suspended mass (30) thus obtained has high mechanical properties, high thickness, the process is wholly compatible with standard microelectronics techniques and can be implemented at low cost.

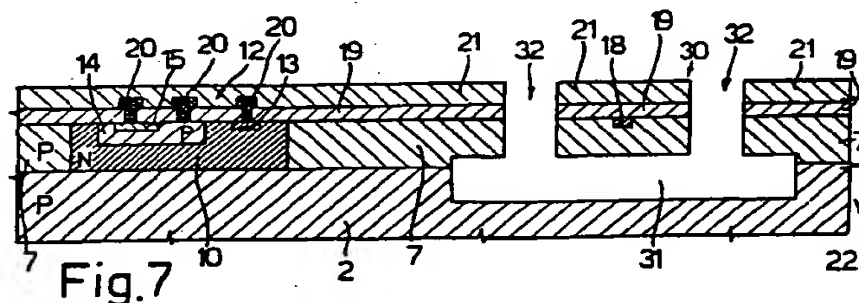


Fig. 7

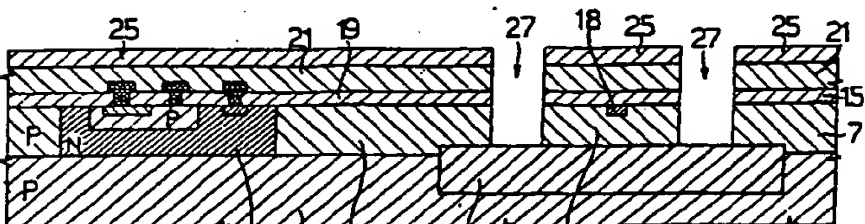
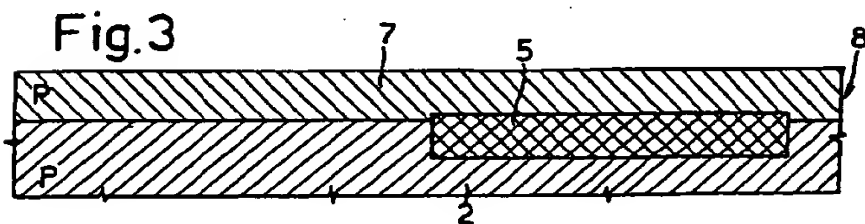


Fig. 6a

EP 0 895 276 A1

of non-exhaustive example, with reference to the accompanying drawings in which:

- Figs. 1-5 show transverse sections through a wafer of semiconductor material in successive manufacturing steps;
- Fig. 6a shows a transverse section similar to that of Figs. 1-5 in a subsequent manufacturing step;
- Fig. 6b shows a transverse section similar to that of Figs. 1-5 in a subsequent manufacturing step according to a variant of Fig. 6a;
- Fig. 7 shows a transverse section similar to the previous ones at the end of manufacture; and
- Fig. 8 shows a top view of the structure of Fig. 7.

[0018] According to an embodiment of the process, with reference to Fig. 1, a mask 3 of silicon carbide having openings 4 at the zones in which a sacrificial layer of porous silicon is to be formed, is formed on top of a wafer 1 of P-type single-crystal silicon with a resistivity of approx. 10-18  $\Omega\text{cm}$  and defining the substrate 2 of the device.

[0019] Subsequently the wafer 1 is subjected to an anodizing process in an electrochemical cell containing an aqueous solution of hydrofluoric acid and ethanol for the formation of porous silicon. An example of an electrochemical cell which can be used for this purpose is described for example in the article by V. Lehmann, "Porous Silicon - A new Material for MEMS", IEEE 1996; this article provides a detailed description of the process to be followed if the chip is N-type; if the chip 1 is P-type, as in the present embodiment, the process is similar but the illumination of the wafer is not required. In particular, the current density required for the formation of porous silicon is between 10 and 100  $\text{mA}/\text{cm}^2$  inclusive depending on the strength of the solution and the concentration of the silicon; in the cell a positive voltage is applied to a platinum electrode and a negative voltage to the wafer 1. In these conditions the current flow between the two electrodes causes the formation of holes on the surface, giving rise to pores. Part of the substrate 2 underneath the opening 4 of the carbide mask 3 thus transforms from single-crystal silicon to porous silicon, forming a porous sacrificial region 5, as shown in Fig. 2.

[0020] The carbide mask 3 is then removed and a P-type epitaxial layer 7 is grown on the wafer 1, forming a wafer 8 (Fig. 3). The possibility of growing a layer of single-crystal silicon of optimum quality epitaxially on layers of porous silicon has recently been demonstrated for devices using SOI substrates, cf. for example C. Oules, A. Halimaoui, J.L. Regolini, A. Perio and G. Bornchil, "Silicon on Insulator Structures Obtained by Epitaxial Growth of Silicon over Porous Silicon", J. Electrochem. Soc., Vol. 139, No. 12, December 1992.

[0021] Conventional standard process steps for forming electronic components of integrated circuits are then carried out; in particular, in the example shown, N-type

pockets 10, extending from the surface 11 of the epitaxial layer 7 as far as the substrate 2 and an NPN transistor 12 equipped with an  $\text{N}^+$ -type collector contact region 12, a P-type base region 14 and an  $\text{N}^+$ -type emitter region 15 are formed in the epitaxial layer 7. At this point, depending on the type of microstructure to be formed and the physical principle on which its operation is based, components or regions necessary for said microstructure may also be formed; in particular, process steps already present for forming the components of the integrated circuit or suitable steps may be used for the purpose.

[0022] Reference will be made below, purely by way of example, to the production of a resonant-type acceleration sensor, which requires two integrated resistors extending at least in part at a suspended structure (shelf) as explained in greater detail below. In this case, therefore, at the same time as the step of implantation and diffusion of the emitter 15 and collector 13 contact regions, such integrated resistors may be formed; only one of them is visible in Fig. 4, denoted by 18. Alternatively, a heater element is formed in the case of a chemoresistive gas sensor, or piezoresistors in the case of a piezoresistive pressure sensor.

[0023] A dielectric layer 19 for forming contact openings of the electronic components of the integrated circuit and components associated with the suspended structure is then deposited, masked and etched on the surface 11 of the epitaxial layer 7; a metal layer for forming contacts 20 and metallic inter-connections is deposited and defined; and a dielectric passivation layer 21 is deposited, thus forming a wafer 22 shown in Fig. 4.

[0024] A resist mask 23 is then formed for the removal of the dielectric layers 19 and 21 in the zone of the contact pads (to permit the electrical contacting of the device, in a way not shown), and in the zone in which the suspended structure is to be formed, forming two openings 24 in the layers 19, 21, as shown in Fig. 5.

[0025] After the removal of the resist mask 23, steps preparatory to the removal of the buried sacrificial layer 5 are carried out. In particular these preparatory steps may be carried out according to two alternative possibilities. According to a first solution, using a suitable carbide mask 25 having openings slightly larger than the resist mask 23 (in a manner not shown), an RIE plasma etching of the epitaxial layer 7 is carried out, which leads to the formation of trenches 27 extending from the surface 11 of the epitaxial layer 7 as far as the porous sacrificial region 5, as shown in Fig. 6a; in this case etching automatically stops on the porous sacrificial region 5. Then, the porous sacrificial region 5 of silicon is oxidized through the trenches 27 (on this subject, see for example the article: "Silicon on Insulator Structures Obtained by Epitaxial Growth of Silicon over Porous Silicon" op. cit.) and forms a first oxidized sacrificial region 28, as shown in Fig. 6a.

[0026] According to the variant of Fig. 6b, the preparatory steps comprise forming a carbide mask 25' wholly

- forming a sacrificial region (28; 29) of porous material inside a body (22) of single-crystal semiconductor material;
  - removing said sacrificial region through openings (27; 7') in said body. 5
2. A process according to Claim 1, characterized in that said step of forming a sacrificial region (28; 29) comprises the steps of: 10
- selectively treating a substrate portion (2) of single-crystal semiconductor material to form a porous semiconductor material portion (5); and
  - subsequently growing an epitaxial layer (7) of single-crystal silicon on said substrate (2). 15
3. A process according to Claim 2, characterized in that said step of selectively treating comprises the steps of: 20
- masking said substrate (2) forming a mask (3) having an opening (4) at said substrate portion;
  - anodizing said substrate portion in an electrochemical cell comprising an anodizing solution. 25
4. A process according to Claim 2 or 3, characterized in that said step of removing said sacrificial region (28; 29) comprises the steps of:
- oxidizing said porous semiconductor material portion (5) to obtain an oxidized porous material portion (28; 29); and 30
  - chemically etching said oxidized porous material portion. 35
5. A process according to Claim 4, characterized in that said step of oxidizing comprises the steps of: removing selective portions of said epitaxial layer (7) on top of said porous semiconductor material portion (5) to form trenches (27) and oxidizing said porous semiconductor material portion through said trenches. 40
6. A process according to Claim 4, characterized in that said step of oxidizing comprises the steps of: masking said epitaxial layer (7) by means of a mask (25') having openings over said porous semiconductor material portion (5); and oxidizing portions of said epitaxial layer disposed underneath said openings to form an oxidized region (29) comprising epitaxial layer oxidized portions (7') and said oxidized porous material portion. 45 50
7. A process according to Claim 6, characterized in that said step of etching comprises the step of removing said epitaxial layer oxidized portions (7'). 55
8. A process according to one of Claims 2-7, charac-

terized in that process steps for forming electronic components (12, 18) in said epitaxial layer and inter-connections (20) are carried out after said step of growing an epitaxial layer (7) and before said step of removing said sacrificial region (28; 29).

9. A process according to Claim 8, characterized in that said process steps comprise the step of implanting resistive elements (18) in said epitaxial layer (7), said resistive elements extending at least partially over said sacrificial region (28; 29) for forming an acceleration microsensor.

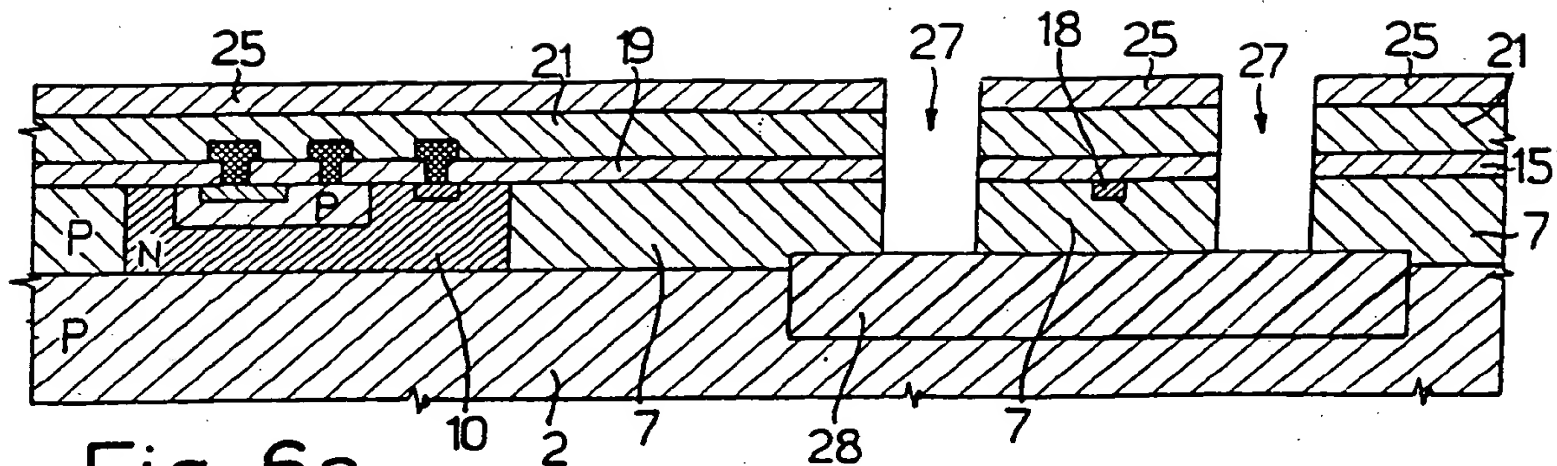


Fig. 6a

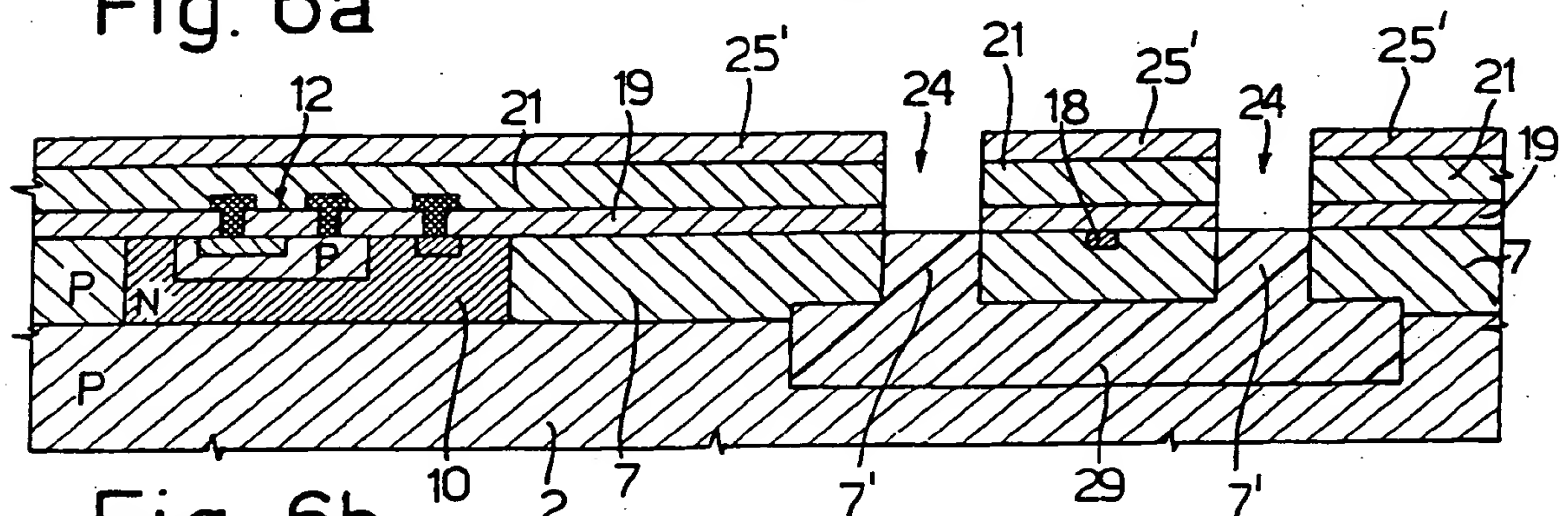


Fig. 6b

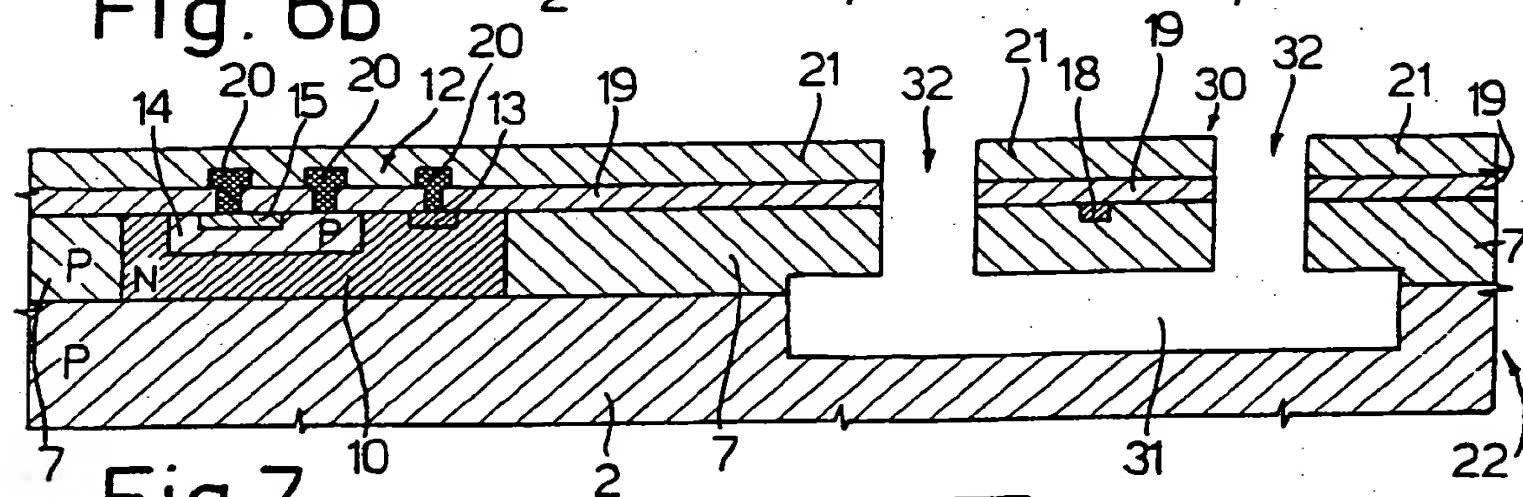


Fig.7

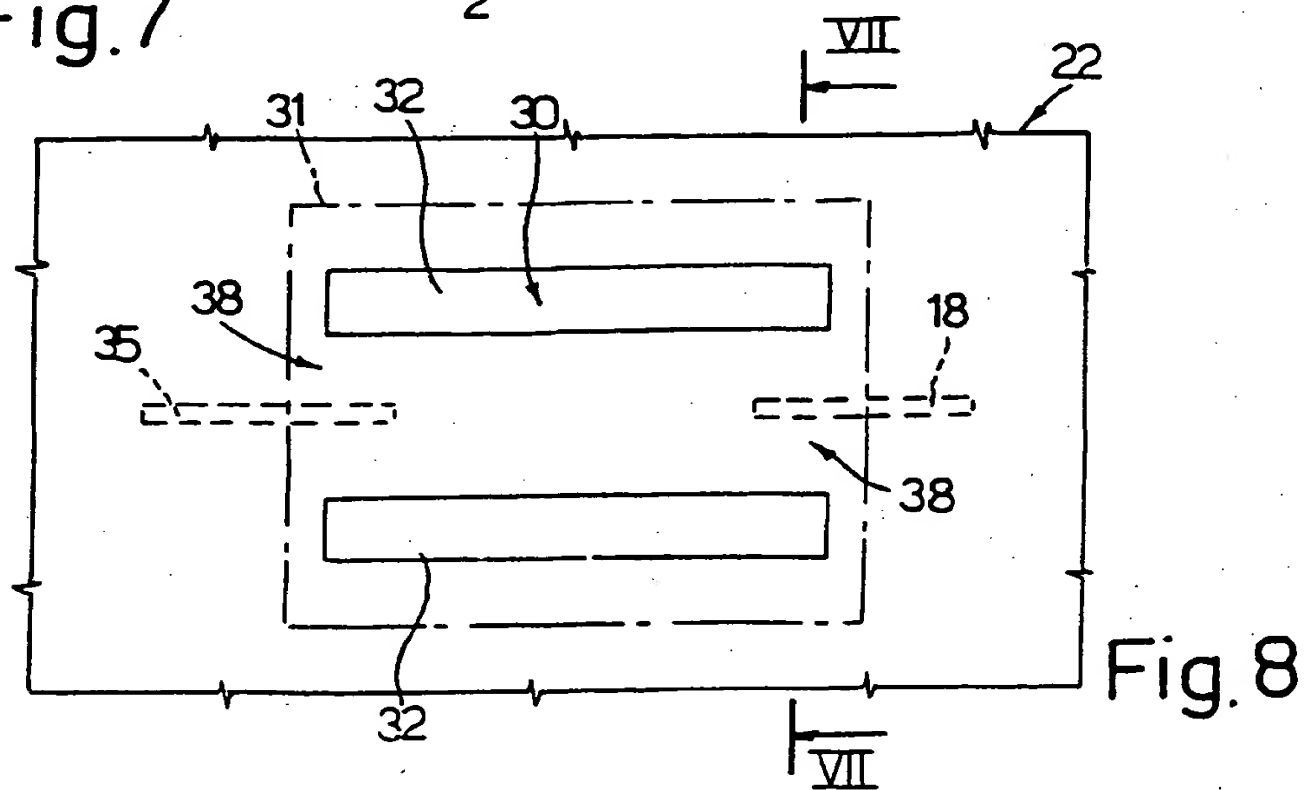


Fig. 8